AMENDMENTS TO THE CLAIMS

Claims 1 – 10 (Canceled)

11. (Currently amended) A method of operating a multi-cache processing unit in a system with multiple processing units, the method comprising:

issuing to multiple cache units of the processing unit, snoops initiated externally with respect to the processing unit;

storing snoop addresses in respective queues of the cache units;

delaying issuance of the snoop addresses that correspond to an externally initiated snoop at least until the cache units have completed prior pending snoop processing; and

supplying a unified response to the system from the processing unit, wherein the unified response is based at least in part on combination of cache responses to externally initiated snoops, wherein the unified response indicates miss if cache responses indicate miss, clean if at least one of the cache responses indicate clean, shared if at least one of the cache responses indicate shared, or dirty if at least one of the cache responses indicate dirty.

12. (Canceled)

13. (Canceled)

14. (Currently amended) The method of ~~claim 12~~ claim 11, further comprising indicating initiators of externally initiated snoops in a common store for the cache.

15. (Original) The method of claim 11, wherein the unified response indicates a cache state for the processing unit that is based at least in part on states of the multiple cache.

16. (Original) The method of claim 15, wherein snoop responses are in accordance with a cache coherency protocol that includes one or more of a MOESI cache coherency protocol, a MESI cache coherency protocol, a MOSI cache coherency protocol, and a MSI cache

coherency protocol.

17. (Canceled).

18. (Original) The method of claim 11 further comprising supplying an internal snoop response to the initiating cache unit.

19. (Original) The method of claim 11 further comprising generating a unified internal snoop response based at least in part on cache responses to an internally initiated snoop and supplying the unified internal snoop response to the initiating cache unit.

20. (Currently amended) ~~The method of claim 11 embodied as a~~ A computer program product ~~encoded~~ encoding instructions in one or more machine-readable media that cause a machine to perform the operations of claim 11.

21. (Currently amended) A method comprising:

determining if a snoop is externally initiated or internally initiated with respect to a domain;
if the snoop is internally initiated,
issuing the snoop from the internal first cache unit that initiates the snoop to an internal second cache unit, wherein the first and second cache units are of the domain,
supplying an internal snoop response from the second cache unit to the first cache unit; and
if the snoop is externally initiated,
issuing the externally initiated snoop to the first and second cache units,
generating a processing unit response based at least in part on responses from the first and second cache units,
indicating the source of the snoop in a first encoding;
indicating the snoop address in snoop queue for the first cache unit and in a snoop queue for the second cache unit;
storing the first supplied cache response from the cache units at least until the second cache response is supplied; and

supplying the processing unit response at least to the source of the externally initiated snoop.

22. (Canceled)

23. (Original) The method of claim 21, wherein snoop responses are in accordance with a cache coherency protocol that includes one or more of a MOESI cache coherency protocol, a MESI cache coherency protocol, a MOST cache coherency protocol, and a MSI cache coherency protocol.

24. (Original) The method of claim 23, wherein the generated processing unit response indicates miss if both cache responses indicate miss, shared if at least one of the cache responses indicate shared, clean if at least one of the cache responses indicate clean, or dirty if at least one of the cache responses indicate dirty.

25. (Original) The method of claim 21 further comprising delaying issuance of the externally initiated snoop at least until the first and second cache units have completed processing of one or more prior pending snoops.

26. (Original) The method of claim 21 further comprising:

issuing the internally initiated snoop to a third internal cache unit;

supplying the internal response to the first internal cache unit, wherein the internal response is based at least in part on the second cache unit's response and the third cache unit's response.

27. (Original) The method of claim 21 further comprising delaying issuance of the snoop if the snoop address overlaps an address of an internal cache miss of a read or write operation at least until arrival of data for the internal cache miss.

28. (Original) The method of claim 21, wherein the domain corresponds to one or more of a processing unit of a multi-processing unit system and a port.

29. (Original) The method of claim 28 wherein the port includes a JBus port.

30. (Original) The method of claim 21 embodied as a computer program product encoded in one or more machine-readable media.

31. (Original) An integrated circuit comprising:

a plurality of cache units, each of the plurality of cache units having at least one cache;

a snoop controller for the integrated circuit, the snoop controller coupled with the plurality of cache units and the snoop controller having, a snoop information store having a plurality of entries, each of the entries to indicate source of a snoop and whether a snoop is being processed;

snoop address stores to indicate addresses of corresponding snoops indicated in the snoop information store, wherein the snoop address stores indicate addresses for respective ones of the plurality of cache units; and

a snoop control logic coupled with the snoop information store and the snoop address stores, the snoop control logic to issue an externally initiated snoop to the plurality of cache units and to combine cache unit snoop responses to an externally initiated snoop.

32. (Original) The integrated circuit of claim 31, wherein indication of snoop source includes one or more of source identifier and whether a snoop is internally initiated or externally initiated.

33. (Original) The integrated circuit of claim 31, wherein the snoop address stores and the snoop information store include first-in-first-out queues.

34. (Original) The integrated circuit of claim 33, wherein the snoop control logic maintains read and write pointers for the snoop information store and the snoop address stores.

35. (Original) The integrated circuit of claim 31 further comprising an internal cache miss store to record internal cache misses of read and write operations, wherein the snoop control logic prevents issuance of snoops with target addresses that overlap addresses indicated in the local miss store, at least until indication that data of the cache misses has arrived.

36. (Original) The integrated circuit of claim 35, wherein the local miss store includes one or more of summing content addressable memory and content addressable memory.

37. (Original) The integrated circuit of claim 31 further comprising a response store to host snoop responses at least until gathered.

38. (Original) The integrated circuit of claim 37 further comprising the snoop controller logic to gather a first cache unit snoop response from the response store with a second cache unit snoop response, and to generate a unified snoop response based at least in part on the first and second cache unit snoop responses.

39. (Original) The apparatus of claim 37, wherein the response store includes entries sufficient to store responses from at most less than all of the plurality of cache units.

40. (Original) The integrated circuit of claim 31, wherein the cache includes one or more of L1 cache, L2 cache, and L3 cache.

Claims 41 – 62 (Canceled)